

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/829,668	BURGER ET AL.	
Examiner		Art Unit		Page 1 of 1
Robert E. Fennema		2183		

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,814,978	03-1989	Dennis, Jack B.	712/201
*	B	US-5,241,635	08-1993	Papadopoulos et al.	712/201
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Fisher, Joseph. "Trace Scheduling: A Technique for Global Microcode Compaction". IEEE Transactions on Computers, Volume C30, Number 7. July, 1981.
	V	Requa, Joseph. McGraw, James. "The Piecewise Data Flow Architecture: Architectural Concepts". IEEE Transactions on Computers, Volume C32, Number 5. May, 1983.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.